DMAC

Media Access Controller

ver 2.07

OVERVIEW

The DMAC is hardware implementation of media access control protocol defined by the IEEE standard. DMAC in cooperation with external PHY device enables network functionality in design. It is capable of transmitting and receiving Ethernet frames to and from the network. Half and full duplex modes are supported, as well 10 and 100 Mbit/s speed. The core is able to work with wide range of processors: 8, 16 and 32 bit data bus, with little or big endian byte order format. Design is technology independent and thus can be implemented in variety of process technologies. This core strictly conforms to IEEE 802.3 standard.

KEY FEATURES

- Conforms to IEEE 802.3-2002 specification
- 8/16/32-bit CPU slave interface with little or big endianess
- Simple interface allows easy connection to CPU
- Narrow address bus with indirect I/O interface to the transmit and receive data dual port memories
- Supports 10BASE-T and 100BASE-TX/FX IEEE 802.3 compliant MII PHYs
- Media Independent Interface (MII) for connection to external 10/100 Mbps PHY transceivers
- Supports full and half duplex operation at 10 Mbps or 100 Mbps
- CRC-32 algorithm calculates the FCS nibble at a time, automatic FCS generation and checking, able to capture frames with CRC errors if required
- Lite design, small gate count and fast operation
- Programmable or fixed MAC address
- Promiscuous mode support
- Dynamic PHY configuration by MII management interface
- Receive FIFO able to store many messages at a time
- Allows operation from a wide range of input bus clock frequencies
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

APPLICATIONS

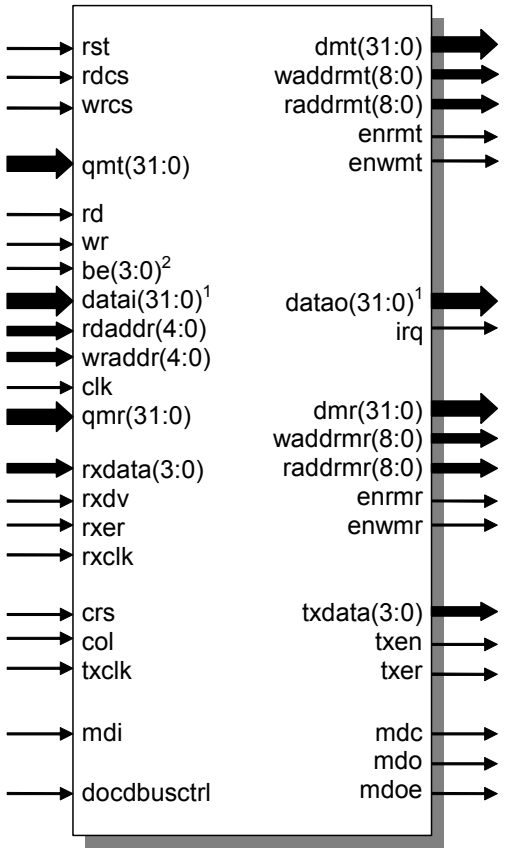
- Embedded microprocessor boards
- Networking devices (Network Interface Cards, routers, switches)
- Communications systems

http://www.DigitalCoreDesign.com
http://www.dcd.pl

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

SYMBOL



1 – data bus can be configured as 8-, 16- or 32- bit depends on processor's bus size

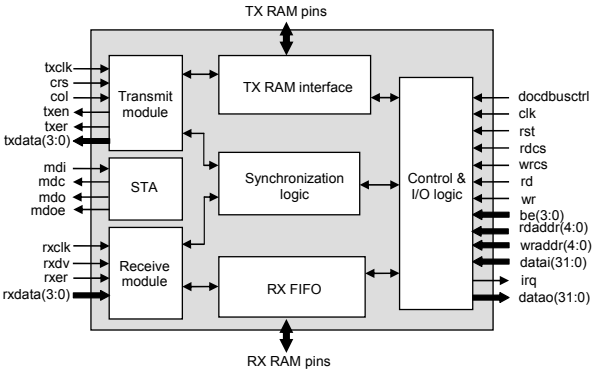
2 – byte enable (be) size is set accordingly to data bus size

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
rdcs	input	Read chip select
wrcs	input	Write chip select
rd	input	Read data strobe
wr	input	Write data strobe
rdaddr(4:0)	input	Host read address bus
wraddr(4:0)	input	Host write address bus
be(3:0) [2]	input	Host byte enable
datai(31:0)[1]	input	Host output data bus
qmr(31:0)	input	RX DPRAM data output
qmt(31:0)	input	TX DPRAM data output
rxdata(3:0)	input	Ethernet receive data
rxdv	input	Ethernet receive data valid
rxer	input	Ethernet receive error
rxclk	input	Ethernet receive clock
txclk	input	Ethernet transmit clock
crs	input	Ethernet carrier sense
col	input	Ethernet collision detection
mdi	input	Management data input
docdbusctrl	input	DoCD debugger input
datao(31:0)[1]	output	Host input data bus
irq	output	Interrupt signal
dmr(31:0)	output	RX DPRAM data input
waddrmr(8:0)	output	RX DPRAM write address
raddrmr(8:0)	output	RX DPRAM read address
enrmr	output	RX DPRAM read enable
enwmr	output	RX DPRAM write enable
dmt(31:0)	output	TX DPRAM data input
waddrmt(8:0)	output	TX DPRAM write address
raddrmt(8:0)	output	TX DPRAM read address
enrmt	output	TX DPRAM read enable
enwmt	output	TX DPRAM write enable
txer	output	Ethernet transmit error
txen	output	Ethernet transmit enable
txdata(3:0)	output	Ethernet transmit data
mdc	output	Management clock
mdo	output	Management data output
mdoe	output	Management data output enable
clk	input	Global clock
rst	input	Global reset
rdcs	input	Read chip select
wrcs	input	Write chip select

BLOCK DIAGRAM

Figure below shows the DMAC IP Core block diagram.



Transmit module – Performs transmit management functions, sends frames to Ethernet medium.

Receive module – is responsible for receiving frames from the Ethernet. Provides necessary functions for frame decapsulation, CRC checking, address recognizing and error detection.

Synchronization logic – There are 3 clock domains in the DMAC core. This module performs synchronization between these.

TX RAM / RX FIFO RAM interfaces – Interfaces to external dual port memories used by the DMAC core to store received and transmitted frames.

Control and I/O logic – This module provides interface to CPU/BUS. It exchanges data and control logic with transmit and receive modules, thus controls these to perform transmit and receive operations.

STA – Station Management entity provides capability to communicate with PHY by simple serial management interface.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F_{max} [MHz] clk / rxclk / txclk
STRATIX II	-3	967 + 4 kB RAM	211 / 200 / 175
CYCLONE II	-6	1222 + 4 kB RAM	150 / 156 / 152
STRATIX GX	-5	1255 + 4 kB RAM	152 / 156 / 138
STRATIX	-5	1255 + 4 kB RAM	162 / 147 / 137
CYCLONE	-6	1254 + 4 kB RAM	148 / 133 / 133
APEX II	-7	1622 + 4 kB RAM	145 / 106 / 111
APEX20KC	-7	1622 + 4 kB RAM	127 / 118 / 117
APEX20KE	-1	1622 + 4 kB RAM	108 / 99 / 111
APEX20K	-1	1622 + 4 kB RAM	86 / 87 / 88

Core performance in ALTERA® devices

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